REMARKS

Claims 1-48 were pending in the present application. Claims xxx have been cancelled. Claims 1, 16, 17, 32, 33, and 48 have been amended. Accordingly, claims 1-48 remain pending in the application.

Claims 6 and 32 stand rejected under 35 U.S.C §112, 2nd paragraph, as being indefinite. Applicant respectfully traverses the rejection of claim 6. More particularly, claim 6 recites "the active device." Claim 6 depends from claim 4, which recites an "additional active device." If claim 6 were referring back to the "additional active device" that is how claim 6 would read. Accordingly, the phrase is not intended to refer back to either the active device or the additional active device. Since claim 6 refers to "the active device," it is clearly referring to the active device that is recited in claim 1. Applicant has amended the claims to overcome the rejection of claim 32. Specifically, claim 32 was amended to depend from claim 22 for antecedent basis. A similar amendment was made to claim 16.

Claims 1-48 stand rejected under 35 U.S.C. §102(b) as being anticipated by Liencres et al. (U.S. Patent No. 5,434,993) (hereinafter " Liencres"). Although Applicant respectfully traverses at least portions of this rejection, Applicant has amended the claims for clarification. Support for the amendment may be found in the detailed description at least at paragraph [0287].

Applicant's claim 1, as amended, recites a system comprising in pertinent part,

> "a node including an active device, an interface to an inter-node network, a memory, and an address network coupling the active device, the interface, and the memory;...
> wherein in response to receiving from the active device an address packet initiating a transaction to gain an access right to a coherency unit, the memory is configured to send data corresponding to the coherency unit to the active device dependent on memory response information associated with the coherency unit, wherein the memory response information includes information used to derive global access state information for the coherency unit;

wherein if the transaction cannot be satisfied within the node, the memory is configured to forward a report corresponding to the address packet to the interface, wherein in response to the report, the interface is configured to send the additional node a coherency message requesting the access right via the inter-node network." (Emphasis added)

The Examiner asserts Liencres teaches each and every limitation recited in Applicant's claim 1. More particularly, the Examiner asserts Liencres teaches the interface to an internode network as being element 31, an address network coupling the active device the interface and the memory as being element 33. In addition, the Examiner asserts Liencres teaches the remaining limitations at col. 7 "read transactions." Applicant respectfully disagrees with the Examiner's characterization of Liencres and the application of Liencres to Applicant's claims.

Specifically, as illustrated in Fig.3a and 3b of Liencres, element 33 cannot be the address network as recited in Applicant's claim 1 because it only couples the bus controller 31 to the processor cache controller 35. It does not couple the active device, the interface, and the memory as recited in claim 1.

However, the above notwithstanding, Applicant further asserts Liencres does not teach or disclose "in response to receiving from the active device an address packet initiating a transaction to gain an access right to a coherency unit, send data corresponding to the coherency unit to the active device dependent on memory response information associated with the coherency unit, wherein the memory response information includes information used to derive global access state information for the coherency unit..." or "if the transaction cannot be satisfied within the node, the memory is configured to forward a report corresponding to the address packet to the interface, wherein in response to the report, the interface is configured to send the additional node a coherency message requesting the access right," as recited in claim 1.

Liencres discloses at col. 7

"Read Transactions
When a memory request by the processor 21 cannot by fulfilled by the data in the processor cache memory 37, the processor cache controller 35 sends a read request packet across the cache bus 33 to the bus cache controller 31. The bus cache controller 31 proceeds to broadcast a corresponding read request packet across the memory bus 25. The read transaction initiated by the bus cache controller 31 consists of two packets: a read request packet sent by the bus cache controller 31 on the memory bus 25 and a read reply packet sent by another device on the memory bus. The read request packet contains the address of the memory requested by the processor cache controller 35 and is broadcast to all entities on the memory bus 25. A device on the memory bus 25 that contains the requested memory address responds to the read request packet with a read reply packet containing the subblock which includes the requested memory address. The read reply packet is generally issued by the main memory 23 except when the desired memory address is "owned" by another processor subsystem 20. In that case, the processor subsystem that owns the subblock must generate a read reply packet with the requested data." (Emphasis added)

From the foregoing, Applicant submits Liencres is teaching the cache controller sending a read request that contains the address to the bus controller, which broadcasts the read request to all devices on the memory bus. Applicant fails to see how this teaches the memory sending the data dependent upon memory response information, or to memory forwarding a report corresponding to the address packet to the interface, wherein in response to the report, the interface is configured to send the additional node a coherency message.

Accordingly, Applicant submits claim 1, along with its dependent claims, patentably distinguishes over Liencres for the reasons given above.

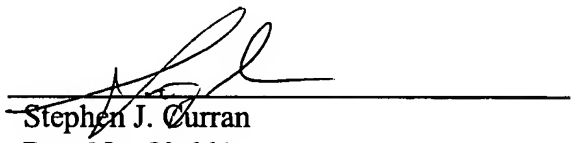
Applicant's claims 17 and 33 recite features that are similar to the features recited in claim 1. Thus Applicant submits claims 17 and 33, along with their respective dependent claims, patentably distinguish over Liencres for at least the reasons given above.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5181-99901/SJC.

Respectfully submitted,



Stephen J. Curran
Reg. No. 50,664
AGENT FOR APPLICANT(S)

Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C.
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 853-8800

Date: March 22, 2007